

IFC



Bhattacharya 1-4-2-2-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**Patent Application**

Applicant(s): R. Bhattacharya et al.

Case: 1-4-2-2-1

Serial No.: 10/620,045

Filing Date: July 15, 2003

Group: 2123

Examiner: To Be Assigned

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature:  Date: July 7, 2005

Title: Method and Apparatus for Automatic Generation  
of Multiple Integrated Circuit Simulation Configuration

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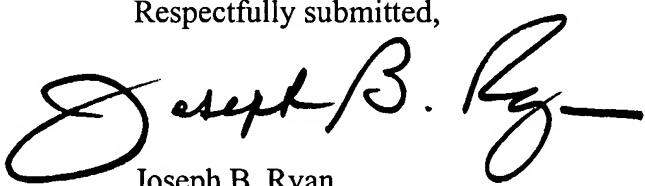
**STATUS REQUEST**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

To date, we have received no communication or official action from the Examiner in charge of the above-identified patent application. Please let us know the status of this case.

Respectfully submitted,



Date: July 7, 2005

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